

# 74HC175; 74HCT175

Quad D-type flip-flop with reset; positive-edge trigger

Rev. 4 — 8 April 2014

Product data sheet

## 1. General description

The 74HC175; 74HCT175 are quad positive edge-triggered D-type flip-flops with individual data inputs (D<sub>n</sub>) and both Q<sub>n</sub> and  $\overline{Q}_n$  outputs. The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition is stored in the flip-flop and appears at the Q output. A LOW on  $\overline{MR}$  causes the flip-flops and outputs to be reset LOW.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

## 2. Features and benefits

- Input levels:
  - ◆ For 74HC175: CMOS level
  - ◆ For 74HCT175: TTL level
- Four edge-triggered D-type flip-flops
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC175N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT175N				
74HC175D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT175D				
74HC175DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT175DB				
74HC175PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT175PW				



## 4. Functional diagram

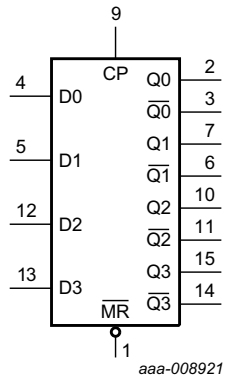


Fig 1. Logic symbol

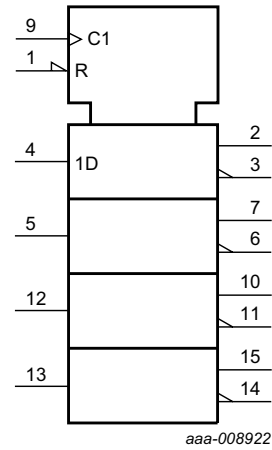


Fig 2. IEC logic symbol

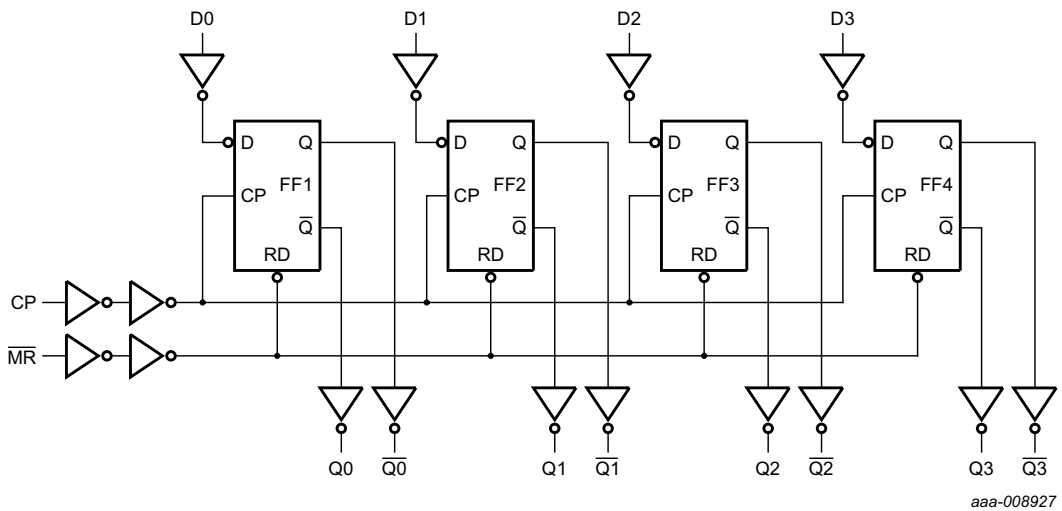
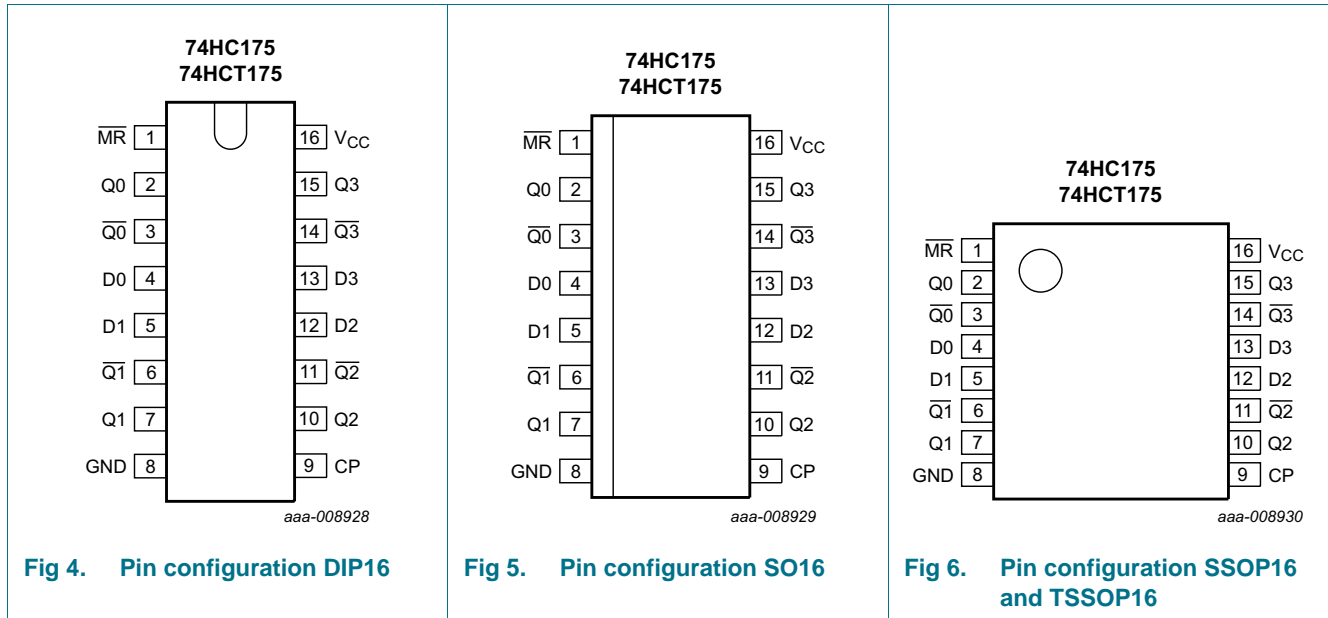


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	asynchronous master reset input (active LOW)
Q0 to Q3	2, 7, 10, 15	flip-flop output
Q0 to Q3	3, 6, 11, 14	complementary flip-flop output
D0 to D3	4, 5, 12, 13	data input
GND	8	ground (0 V)
CP	9	clock input (LOW-to-HIGH edge-triggered)
VCC	16	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating modes	Inputs			Outputs	
	$\overline{\text{MR}}$	CP	Dn	Qn	$\overline{\text{Qn}}$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition.

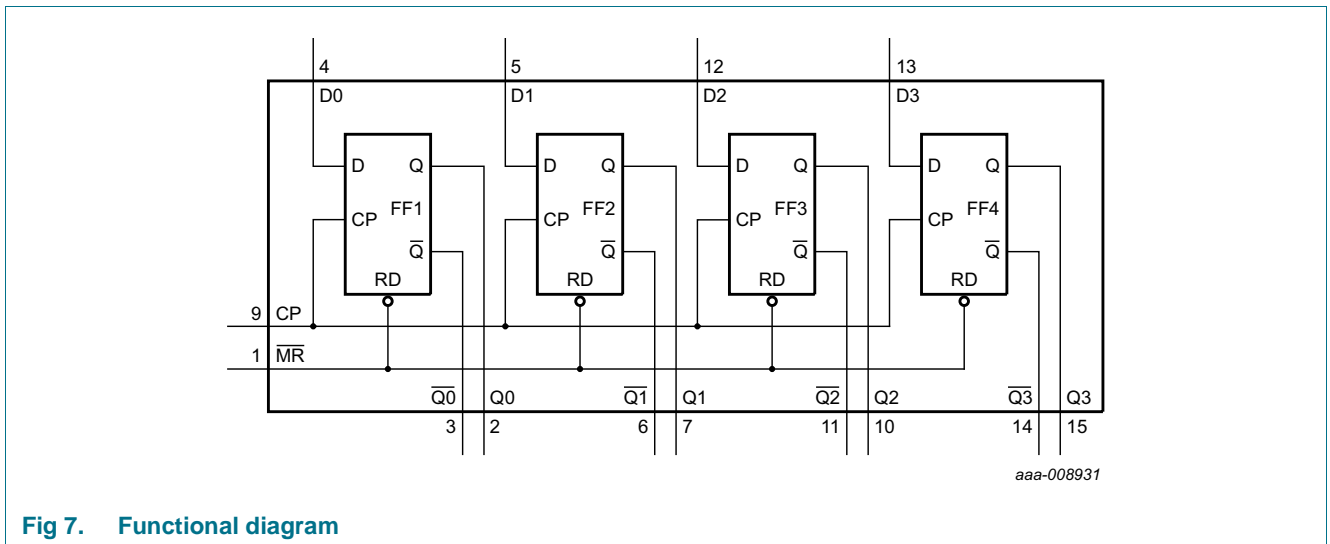


Fig 7. Functional diagram

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	±20	mA
$I_O$	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		DIP16 package [1]	-	750	mW
		SO16, SSOP16 and TSSOP16 [2]	-	500	mW

- [1] For DIP16 package: above 70 °C the value of P<sub>tot</sub> derates linearly with 12 mW/K.
- [2] For SO16 package: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
For SSOP16 and TSSOP16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC175			74HCT175			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC175</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
	I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V	

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT175</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		Dn input	-	40	144	-	180	-	196	μA
		CP input	-	60	216	-	270	-	294	μA
		MR input	-	100	360	-	450	-	490	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 11](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC175</b>										
$t_{pd}$	propagation delay	CP to Qn, $\overline{Qn}$ ; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
$t_{PHL}$	HIGH to LOW propagation delay	$\overline{MR}$ to Qn, $\overline{Qn}$ ; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
$t_t$	transition time	Qn output; see <a href="#">Figure 8</a> <sup>[2]</sup>								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
$t_w$	pulse width	CP input HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
		$\overline{MR}$ input LOW; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0$ V	80	19	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	ns	
$t_{rec}$	recovery time	$\overline{MR}$ to CP; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0$ V	5	-33	-	5	-	5	-	ns
		$V_{CC} = 4.5$ V	5	-12	-	5	-	5	-	ns
		$V_{CC} = 6.0$ V	5	-10	-	5	-	5	ns	
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0$ V	80	3	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	1	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	1	-	17	-	20	ns	

**Table 7. Dynamic characteristics ...continued**  
 GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 11](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit		
			Min	Typ	Max	Min	Max	Min	Max			
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Figure 8</a>										
		V <sub>CC</sub> = 2.0 V	25	2	-	30	-	40	-	ns		
		V <sub>CC</sub> = 4.5 V	5	0	-	6	-	8	-	ns		
		V <sub>CC</sub> = 6.0 V	4	0	-	5	-	7	-	ns		
f <sub>max</sub>	maximum frequency	CP input; see <a href="#">Figure 8</a>										
		V <sub>CC</sub> = 2.0 V	6	25	-	4.8	-	4	-	MHz		
		V <sub>CC</sub> = 4.5 V	30	75	-	24	-	20	-	MHz		
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	83	-	-	-	-	-	MHz		
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[3]</a>	-	32	-	-	-	-	-	pF		
		<b>74HCT175</b>										
		t <sub>pd</sub>	propagation delay	CP to Qn, $\overline{Qn}$ ; see <a href="#">Figure 8</a> <a href="#">[1]</a>								
				V <sub>CC</sub> = 4.5 V	-	19	33	-	41	-	50	ns
V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-			16	-	-	-	-	-	ns		
t <sub>PHL</sub>	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see <a href="#">Figure 10</a>										
		V <sub>CC</sub> = 4.5 V	-	22	38	-	48	-	57	ns		
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns		
		$\overline{MR}$ to $\overline{Qn}$ ; see <a href="#">Figure 10</a>										
		V <sub>CC</sub> = 4.5 V	-	19	35	-	44	-	53	ns		
t <sub>t</sub>	transition time	Qn output; see <a href="#">Figure 8</a> <a href="#">[2]</a>										
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns		
t <sub>w</sub>	pulse width	CP input; see <a href="#">Figure 8</a>										
		V <sub>CC</sub> = 4.5 V	20	12	-	25	-	30	-	ns		
		$\overline{MR}$ input LOW; see <a href="#">Figure 10</a>										
t <sub>rec</sub>	recovery time	$\overline{MR}$ to CP; see <a href="#">Figure 10</a>										
		V <sub>CC</sub> = 4.5 V	5	-10	-	5	-	5	-	ns		
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 8</a>										
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns		
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Figure 8</a>										
		V <sub>CC</sub> = 4.5 V	5	0	-	5	-	5	-	ns		

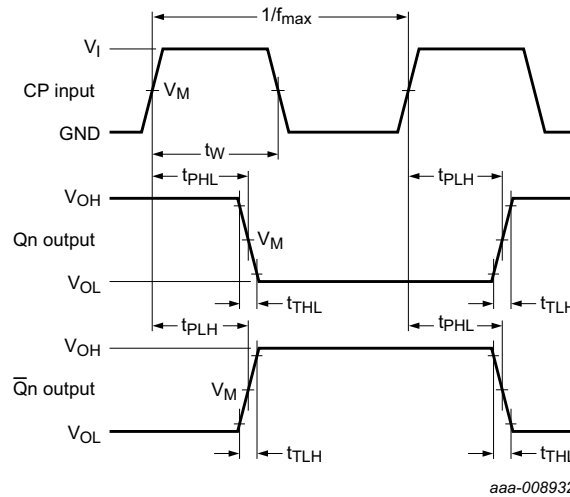


**Table 7. Dynamic characteristics ...continued**  
 GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see [Figure 11](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{max}}$	maximum frequency	CP input; see <a href="#">Figure 8</a>								
		$V_{\text{CC}} = 4.5 \text{ V}$	25	49	-	20	-	17	-	MHz
		$V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	54	-	-	-	-	-	MHz
$C_{\text{PD}}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{\text{CC}} - 1.5 \text{ V}$	[3]	34	-	-	-	-	-	pF

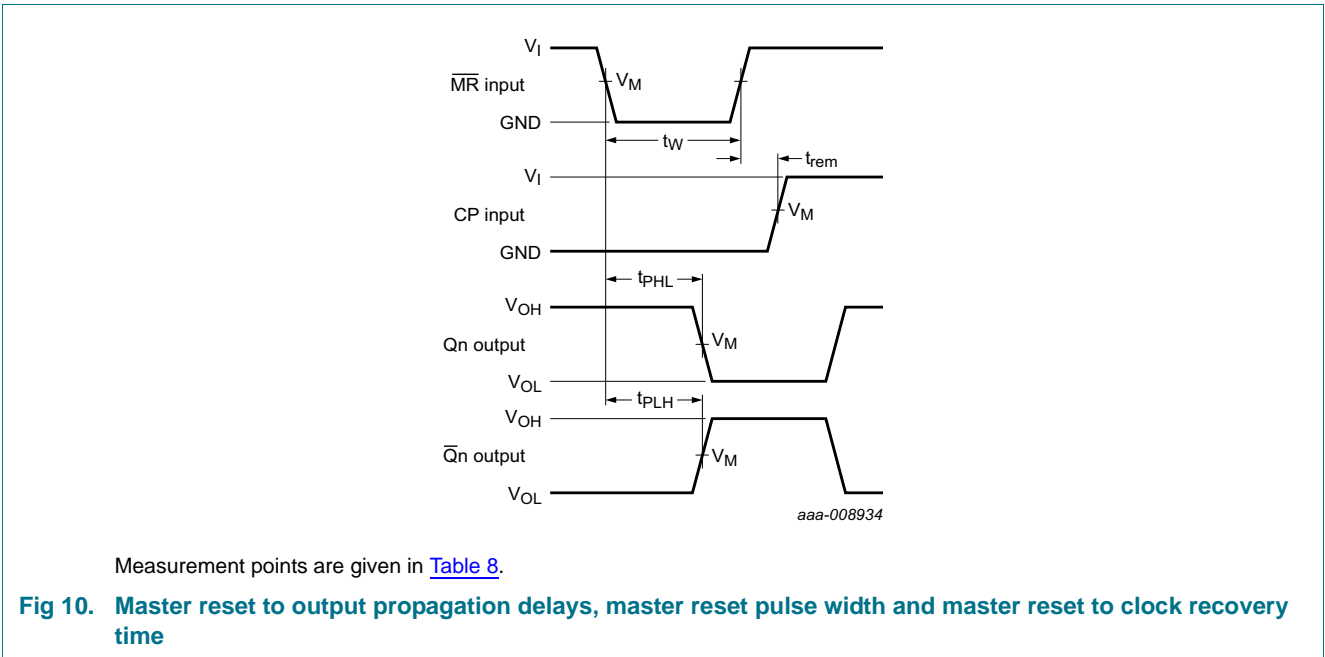
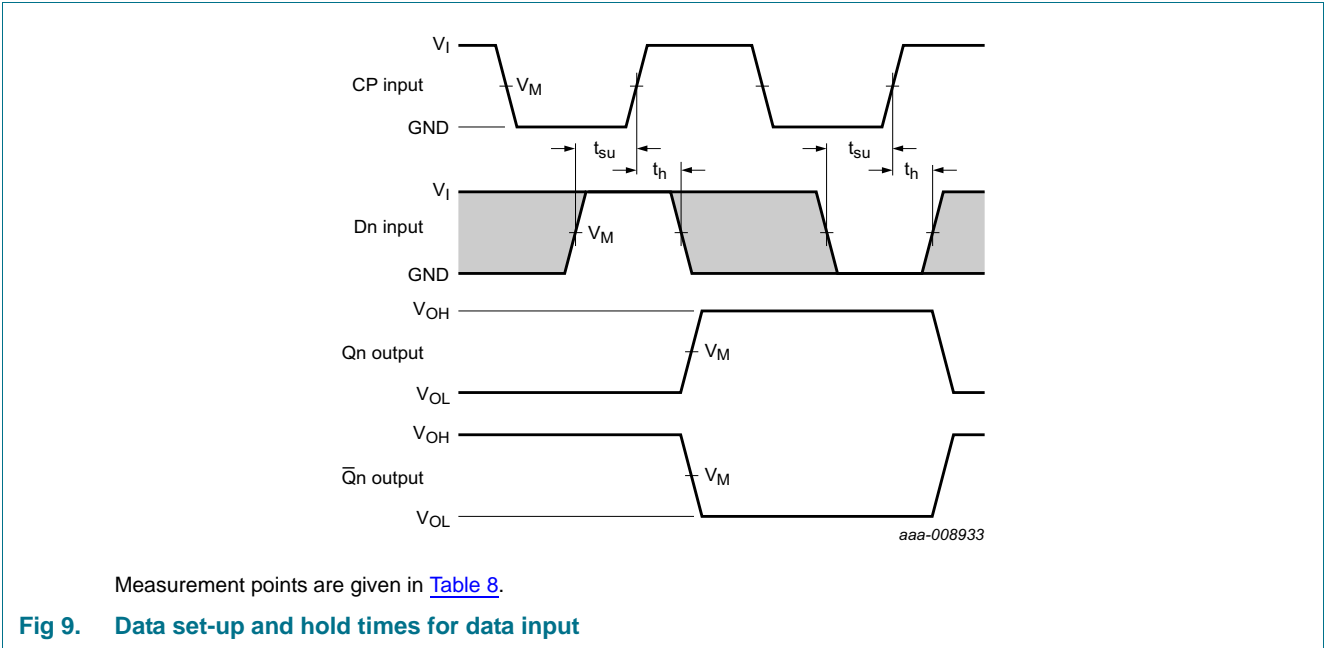
- [1]  $t_{\text{pd}}$  is the same as  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$ .
- [2]  $t_t$  is the same as  $t_{\text{THL}}$  and  $t_{\text{TLH}}$ .
- [3]  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i + \Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $\Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of outputs;  
 $C_L$  = output load capacitance in pF;  
 $V_{\text{CC}}$  = supply voltage in V.

## 11. Waveforms



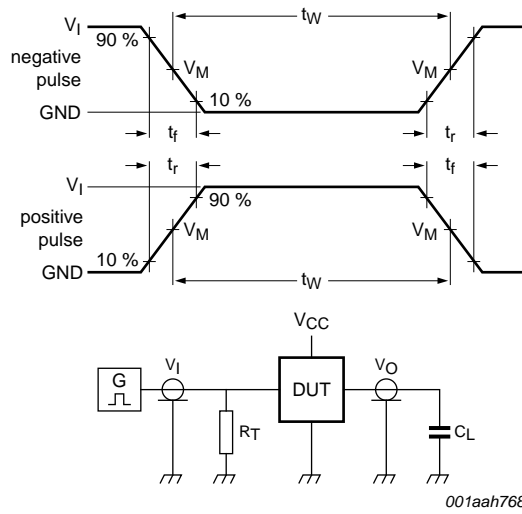
Measurement points are given in [Table 8](#).

**Fig 8. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency**



**Table 8. Measurement points**

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74HC175	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT175	3 V	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

**Fig 11. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load		Test
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
74HC175	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	$t_{PLH}, t_{PHL}$
74HCT175	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	$t_{PLH}, t_{PHL}$

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

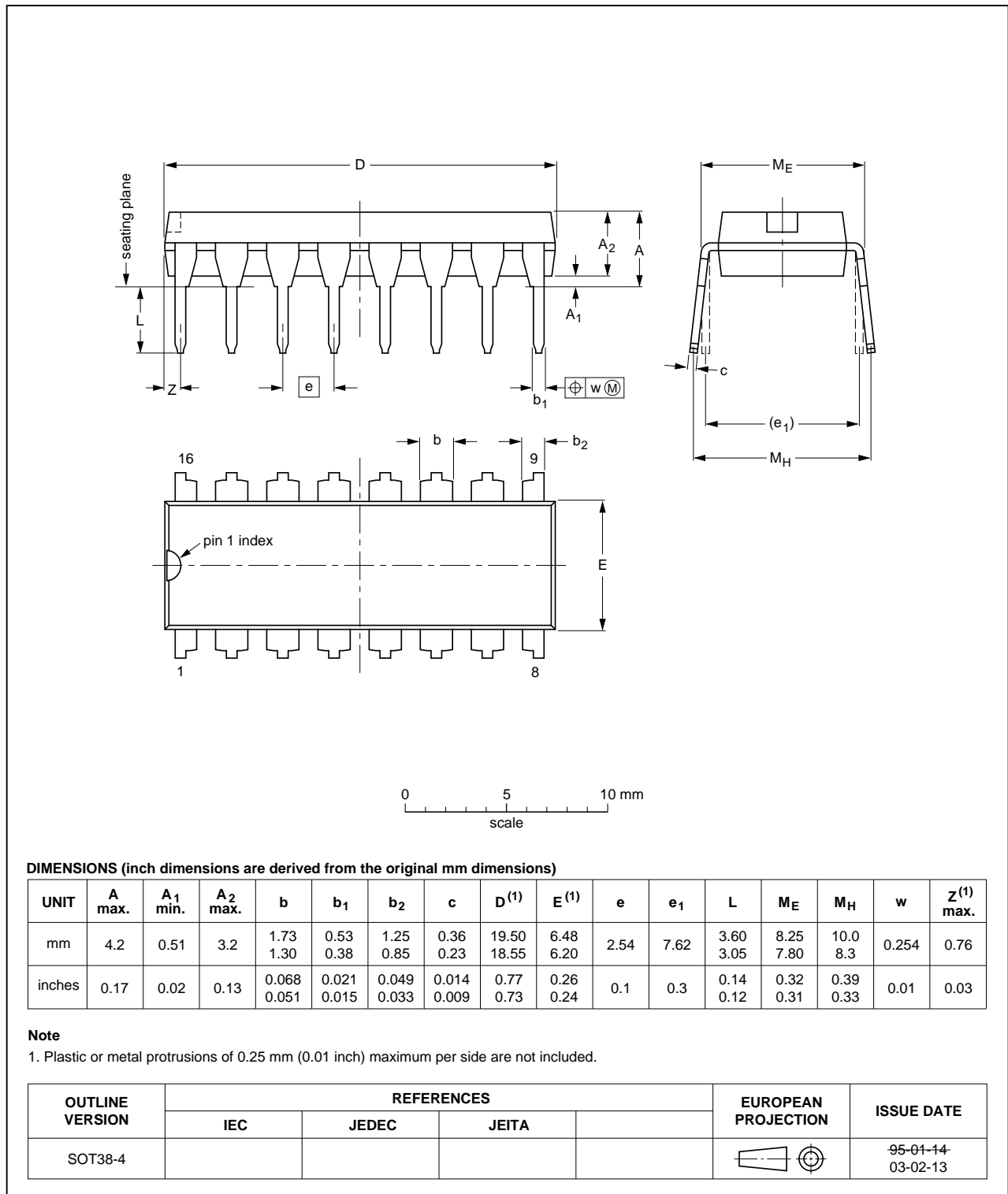


Fig 12. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

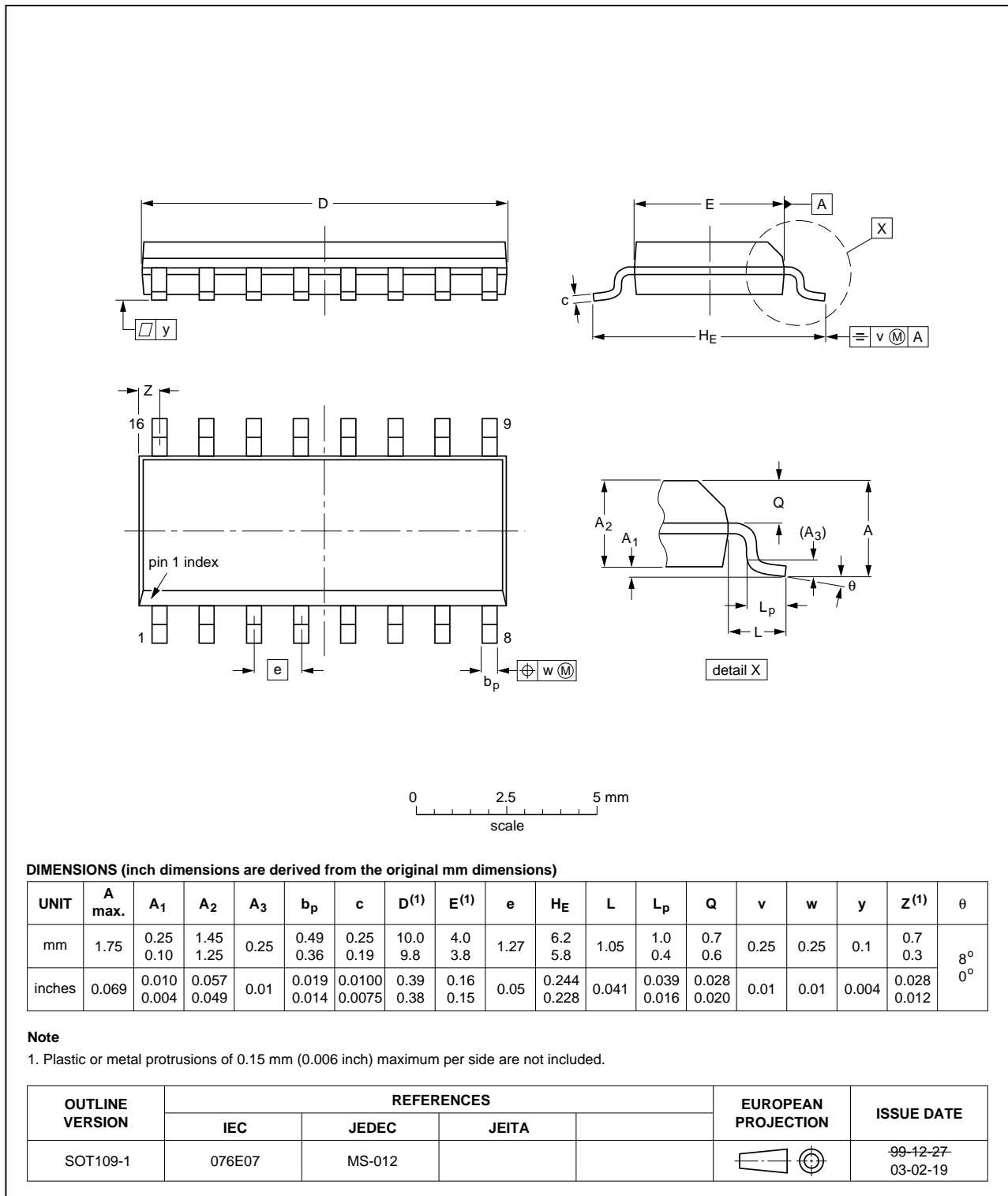


Fig 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

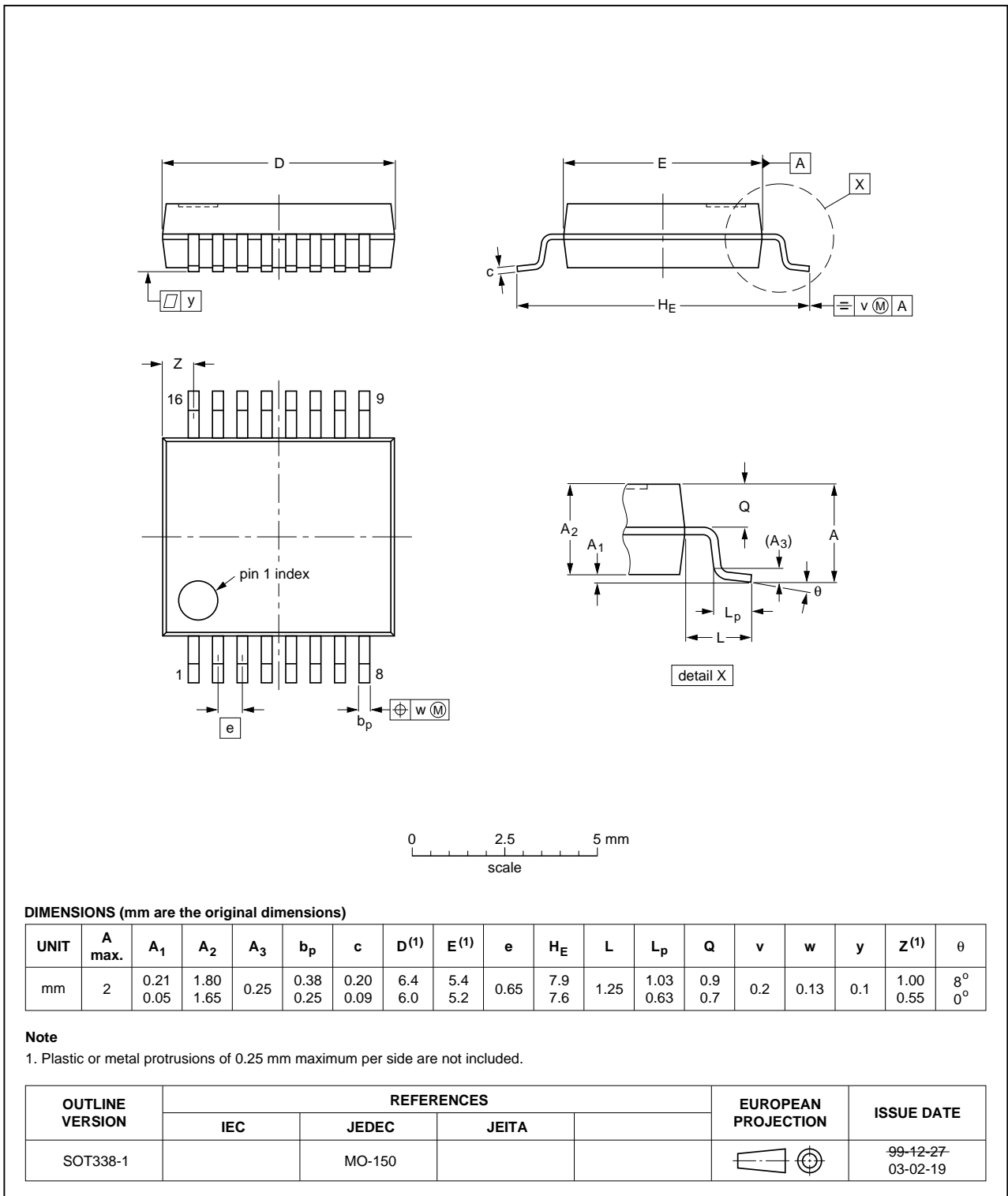


Fig 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

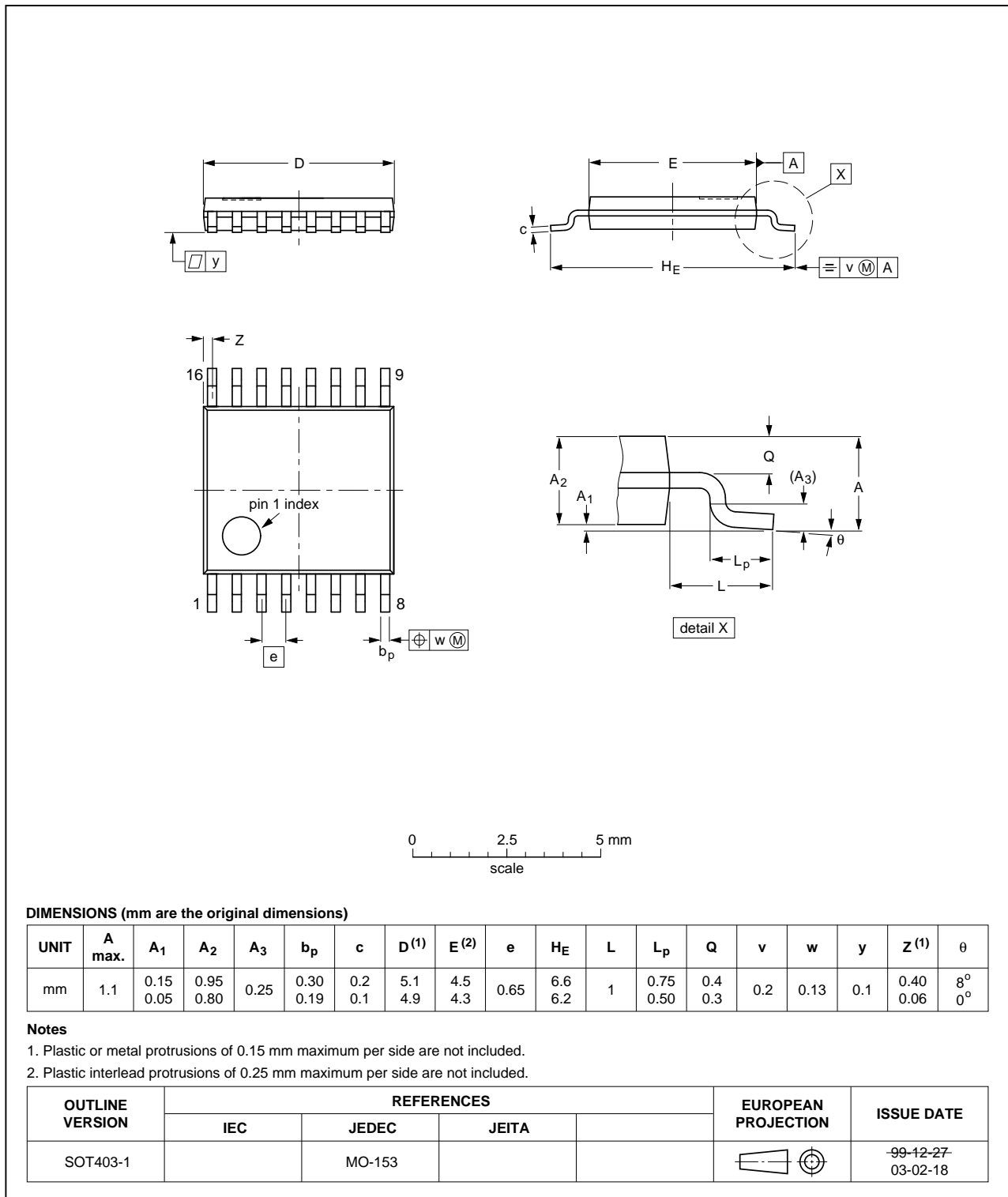


Fig 15. Package outline SOT403-1 (TSSOP16)

### 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

### 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT175 v.4	20140408	Product data sheet	-	74HC_HCT175 v.3
Modifications:	<ul style="list-style-type: none"> <li>General description corrected (errata).</li> </ul>			
74HC_HCT175 v.3	20140331	Product data sheet	-	74HC_HCT175_CNV_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT175_CNV_2	19980708	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 8 April 2014

Document identifier: 74HC\_HCT175